AF 2811

BRINKS HOFER GILSON & LIONE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of: HERNER ET AL.

Appln. No.: 09/928,975

Filed: August 13, 2001

For: LOW RESISTIVITY TITANIUM SILICIDE ON HEAVILY DOPED SEMICONDUCTOR

Attorney Docket No: 10519/57

Examiner: T. MAGEE

Art Unit: 2811

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL

Sir:

Attached is/are:

☒ Amended Supplemental Appeal Brief (11 pages).

☒ Return Receipt Postcard

Fee calculation:

☐ No additional fee is required.

☐ Small Entity.

☐ An extension fee in an amount of $_____ for a _____-month extension of time under 37 C.F.R. § 1.136(a).

☐ A petition or processing fee in an amount of $_____ under 37 C.F.R. § 1.17(_____).

☐ An additional filing fee has been calculated as shown below:

						Small Entity			Not a Small Entity	
	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra		Rate	Add'l Fee	or	Rate	Add'l Fee
Total		Minus				x $25=			x $50=	
Indep.		Minus				x 100=			x $200=	
First Presentation of Multiple Dep. Claim						+$180=			+ $360=	
						Total	$		Total	$

Fee payment:

☐ A check in the amount of $_____ is enclosed.

☐ Please charge Deposit Account No. 23-1925 in the amount of $_____. A copy of this Transmittal is enclosed for this purpose.

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☒ The Director is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this paper (including any extension fee required to ensure that this paper is timely filed), or to credit any overpayment, to Deposit Account No. 23-1925.

Respectfully submitted,

11-15-05
Date

Joseph F. Hetz (Reg. No. 41,070)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on November 15, 2005
Date of Deposit

Joseph F. Hetz - Reg. No. 41,070
Name of Applicant, Assignee or Registered Representative

Signature

Our Case No. 10519-57

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Herner et al.	Examiner:	T. Magee
Serial No.:	09/928,975	Group Art Unit:	2811
Filed:	August 13, 2001		
For:	Low Resistivity Titanium Silicide on Heavily Doped Semiconductor		

AMENDED SUPPLEMENTAL APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In their Supplemental Appeal Brief, Applicants incorporated by reference arguments regarding Claims 7 and 8 presented in their previously-filed appeal brief. A Notification of Non-Compliant Appeal Brief mailed November 7, 2005 pointed out that those arguments contained an argument regarding Wilson et al., which was no longer being applied against those claims. In response to the Notification, Applicants submit this Amended Supplemental Appeal Brief, which removes the arguments regarding Wilson et al. from Claims 7 and 8.

TABLE OF CONTENTS

I. Real Party in Interest

Matrix Semiconductor, Inc. is the real party in interest.

II. Related Appeals and Interferences

The appeal in U.S. patent application serial number 10/247,071, filed September 18, 2002, which is a divisional of the present application, may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-8 are pending and the subject of this appeal.

IV. Status of Amendments

Subsequent to the final rejection, Applicants filed an Amendment on October 9, 2003. That Amendment was acted upon by the Examiner and was denied entry.

V. Summary of Invention

Applicants incorporate by reference the Summary of Invention presented in the previously-filed appeal brief.

VI. Issues

There are three issues presented in this appeal:

1. Whether Claims 1-6 are unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al.[1], Spinelli et al.[2], and Nakayama et al.[3];

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[1] U.S. Patent Application No. US 2002/0045342A1.

[2] Spinelli et al., "An Improved Formula for the Determination of the Polysilicon Doping," IEEE Electron Device Letters, vol. 22, no. 6, pages 281-283 (June 2001).

[3] Nakayama et al., "Excellent Process Control Technology for Highly Manufacturable and High Performance 0.18 μm CMOS LSIs," IEEE Digest Tech. Papers, Symposium on VLSI Technology, pages 146-147 (1998).

2. Whether Claim 7 is unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al., Spinelli et al., and Nakayama et al.; and

3. Whether Claim 8 is unpatentable under 35 U.S.C. § 103(a) over the proposed combination of Hu et al., Spinelli et al., Nakayama et al., and Tsukude et al.[4]

VII. Grouping of Claims

Applicants identify the grouping of the claims as follows:

Group I: Claims 1-6. Claims 1-6 do not stand or fall together.

Group II: Claim 7

Group III: Claim 8

VIII. Argument

A. Claim 1 Is Patentable over the Applied References

Independent Claim 1 recites a semiconductor structure with first and second semiconductor regions and a titanium layer. Claim 1 also recites a relationship between the thickness of the second semiconductor region (t1) and the thickness of the titanium layer (t2), specifically:

> t1/t2 being sufficiently small that, when the [titanium] layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region; [and]
>
> t1/t2 being sufficiently large that, when the [titanium] layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide anneals to a phase with a sheet resistance less than 3 ohms/square.

In the new ground of rejection presented in the Office Action, the Examiner stated that these limitations were not given patentable weight because the Examiner considered them to be

[4] Tsukude et al., "A 256 Mb DRAM," Advance Magazine, Mitsubishi Electric, Vol. 75, pages 5-8 (June 1996).

product-by-process limitations. Applicants respectfully submit that these limitations are not product-by-process limitations and should be given patentable weight.

"A product-by-process claim . . . is a product claim that defines the claimed product in terms of the process ***by which it is made***" (emphasis added). MPEP 2173.05(p). Independent Claim 1 is not a product-by-process claim because the elements at issue in Claim 1 define the claimed semiconductor structure in terms of structural limitations (thicknesses of the second semiconductor region and the titanium layer) — not the process by which the semiconductor structure is made. Applicants believe the confusion regarding this claim lies in that the recited thicknesses are defined by what might be misinterpreted as process steps (that when the second semiconductor region reacts with the titanium layer, titanium disilicide is formed having certain characteristics). However, "apparent 'process' terms should be interpreted as structural limitations when used in an adjective non-process sense and define a physical characteristic of the apparatus." *See CVI/Beta Ventures, Inc. v. Custom Optical Frames, Inc.*, 893 F. Supp. 508, 519 (D. Md. 1995).[5] In Claim 1, the "apparent process terms" define a physical characteristic of the claimed semiconductor structure (thicknesses of the second semiconductor region and the titanium layer) and not the process by which the claimed semiconductor structure is made.

Applicants note that Claim 1 is similar to a claim that the Federal Circuit found ***not*** to be a product-by-process claim. In *Union Carbide Chemicals & Plastic Technology Corp. v. Shell Oil Co.*, 308 F.3d 1167 (Fed. Cir. 2002), the claim at issue recited a catalyst comprising silver in a first amount, cesium in a second amount, and an alkali metal in a third amount. The claim further recited that the relation between the amount of silver and the amounts of cesium and the

[5] *See* Chisum on Patents, Section 8.05[4] — Distinguishing Process and Structural Limitations, page 8-172 (Sept. 2003) ("Certain apparent 'process' words in claims are interpreted as structural limitations when they are used in an adjective non-process sense and adequately define a physical characteristic of the product.")

alkali metal were "sufficient to provide an efficiency of ethylene oxide manufacture that is greater than the efficiencies obtainable" when other amounts are used. The claim also recited that the combination of silver, cesium, and the alkali metal was characterizable by a specific efficiency equation. The Court held that the claim was ***not*** a product-by-process claim.

Pending Claim 1 is similar to the claim in *Union Carbide* in that both claims recite an apparent process term that is used in an adjective non-process sense to define a physical characteristic of the claimed product rather than to specify the process by which the claimed product is made. In *Union Carbide*, the claim defines amounts of certain components in terms of an ability to use those components to obtain a manufacture of ethylene oxide with certain characteristics. Similarly, pending Claim 1 defines thicknesses of the second semiconductor region and the titanium layer in terms of an ability to form titanium disilicide with certain characteristics. Both claims are not product-by-process claims.

In summary, Applicants respectfully submit that all elements recited in Claim 1 should be given patentable weight since they are structural limitations — not product-by-process limitations. When all elements in Claim 1 are given patentable weight, the proposed combination fails to yield each and every recited element, as discussed in the arguments made in the previously-filed appeal brief, which are hereby incorporated by reference. Because Claim 1 is patentable over the proposed combination, Applicants respectfully request removal of the rejections of independent Claim 1 and its dependent claims.

B. Claims 2-6 Are Patentable over the Applied References

Claims 2-4 recite specific relationships between t1 and t2, and these relationships were not given patentable weight in the Office Action. For the reasons set forth above with respect to Claim 1, Applicants respectfully submit that these relationships should be given patentable weight since they are structural limitations — not product-by-process limitations. When all elements in Claims 2-4 are given patentable weight, the proposed combination fails to yield each and every recited element, as discussed in the arguments made in the previously-filed appeal brief, which are hereby incorporated by reference. Claims 5 and 6 are also patentable over the proposed combination for the reasons discussed in the previously-filed appeal brief. These reasons are also hereby incorporated by reference. Accordingly, Applicants respectfully request that the rejections of Claims 2-6 be removed.

C. Claim 7 Is Patentable over the Applied References

Group II contains independent Claim 7, which recites a semiconductor structure comprising a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$ and a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, with each conductor having a width no greater than 0.3 μm and at least 90% of the conductors characterized by a sheet resistance less than 3 ohms/square. Claim 7 was rejected in view of the same proposed combination used to reject Claim 1. Applicants respectfully submit that, like Claim 1, Claim 7 is patentable over the applied references.

In both the embodiment in Hu et al. that relates to low resistivity, fine-line titanium silicide and in Nakayama et al., there is no teaching of a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$. Finally, there is no disclosure of

titanium silicide in Spinelli et al. As a result, when the individual references are combined together, the combination, as a whole, fails to teach each and every element recited in independent Claim 7. Accordingly, Applicants respectfully request that the rejections of independent Claim 7.

D. Claim 8 Is Patentable over the Applied References

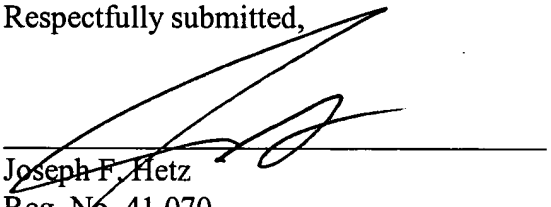
Group III contains Claim 8, which depends from Claim 1 or 7 and recites that the semiconductor structure comprises a 3-D memory array comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip. In the Office Action, it was admitted that the proposed combination of Hu et al., Nakayama et al., and Spinelli et al. fails to teach this element. In an attempt to cure this deficiency, it was proposed to add Tsukude et al. to the combination. However, Tsukude et al. merely teaches a stacked-capacitor memory cell. In other words, Tsukude et al. teaches a memory *cell* that has stacked components — not a memory *array* with individual memory cells stacked vertically above one another in a single chip, as recited in Claim 8. Accordingly, even if Tsukude et al. were added to the other references, the proposed combination still fails to yield the claimed invention.

IX. Conclusion

For the reasons set forth above, Applicants respectfully submit that (1) Claims 1-6 are patentable over the proposed combination of Hu et al., Spinelli et al., and Nakayama et al.; (2) Claim 7 is patentable over the proposed combination of Hu et al., Spinelli et al., and Nakayama et al.; and (3) Claim 8 is patentable over the proposed combination of Hu et al., Spinelli et al., Nakayama et al., and Tsukude et al. Accordingly, removal of the rejections is respectfully requested.

Dated: November 15, 2005

Respectfully submitted,



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X. Appendix

1. A semiconductor structure comprising:

a first semiconductor region characterized by a dopant concentration greater than $1x10^{19}/cm^3$;

a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{19}/cm^3$ and a thickness t1; and

a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than 0.3μm and a thickness t2, wherein $t1 > 1.2t2$;

t1/t2 being sufficiently small that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide is in ohmic contact with the first semiconductor region;

t1/t2 being sufficiently large that, when the layer is reacted with the second semiconductor region to form titanium disilicide, the titanium disilicide anneals to a phase with a sheet resistance less than 3 ohms/square.

2. The semiconductor structure of Claim 1 wherein $t1 \geq 2.2t2$.

3. The semiconductor structure of Claim 1 wherein $t1 = 2.3t2, \pm 0.1t2$.

4. The semiconductor structure of Claim 1 wherein t1 is about 600Å and t2 is about 250Å.

5. The semiconductor structure of Claim 1 wherein the dopant concentration of the first semiconductor region is greater than $1x10^{20}/cm^3$.

6. The semiconductor structure of Claim 1 or 5 wherein the first semiconductor region is doped primarily with boron.

7. A semiconductor structure comprising:

a first semiconductor region characterized by a boron dopant concentration greater than $1x10^{20}/cm^3$; and

a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, each said conductor characterized by a width no greater than 0.3μm, and at least 90% of said conductors characterized by a sheet resistance less than 3 ohms/square;

wherein the set of titanium silicide conductors is formed, in part, by a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1x10^{18}/cm^3$.

8. The semiconductor structure of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array, wherein the 3-D memory array comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip.